COPY

FTQ:SMO44(10-01 Approved for uppersonable 10/31/2002, CMG 451-000 Approved for uppersonable 10/31/2002, CMG 451-000

Substitute for form 1449APTO	Under the Pappment Reduction has of 1995, no parsons are required to respect to a subsection of information between a contains a vigid Olds control not Complete if Known		
INFORMATION DISCLOSURE	Application Number	10/612293	
STATEMENT BY APPLICANT	Filing Date	June 30, 2003	
Cose as many sheets as necessary	First Named Inventor	Day, Daniel	
APR 2 3-2004 gg	- Group Art Unit	2857	
\z	Examiner Name	Unknown	
Sheet 1 of 1 Attorney Docket No: 884.879US1			

US PATENT DOCUMENTS						
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date if Appropriate
1756	US-5,396,501	03/07/1995	Sengoku, Shoichiro	371	22	09/30/1992
77.	US-6,122,762	09/19/2000	Kim, Ho-Ryong	714	726	09/15/1998
- 1	US-6,446,230	09/03/2002	Chung, Sung \$.	714	726	09/14/1998
me	US-6,449,755	09/10/2002	Beausang, James, et al.	716	5	07/14/2000

FOREIGN PATENT DOCUMENTS						
Examiner initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²

	OTHE	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No 1	include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T
pruc		"Boundary Scan (JTAG) Tools and Circuit Board Test Solutions", www.acculogic.com/Products/BoundaryScanHome.htm, 2 pages	
Mur		"Designing for On-Board Programming Using the IEEE 1149.1 (JTAG) Access Port", Intel AP-630 Application Note, Intel order no. 292186-002, available from http://www.intel.com, (November 1996),14 pages	
3mC	-,	"Joint Test Action Group from FOLDOC", <u>Available from</u> http://wombat.doc.ic.ac.uk/foldoc/foldoc.cqi?Joint+Test+Action+Group , (11/15/1999),1 page	
The		"The New Vanguard 330 From Integrated Measurement Systems Offers Cost- Effective Validation of High Performance Logic ICs", www.engineerlng-uk.co.uk, (04/24/2001),2 Pages	

EXAMINER DATE CONSIDERED 2/1/06

Septimize Cisalower Stylement Form (PTQ-1449)

EXAMINER: with all reference special whether or not startion like conformance with NPEP 603, Draw the tribulgh cisalon is not formance and not considered, include copy of this form with next continued to the policient is a place a creck mark need it English tanguage Translation is adjusted.